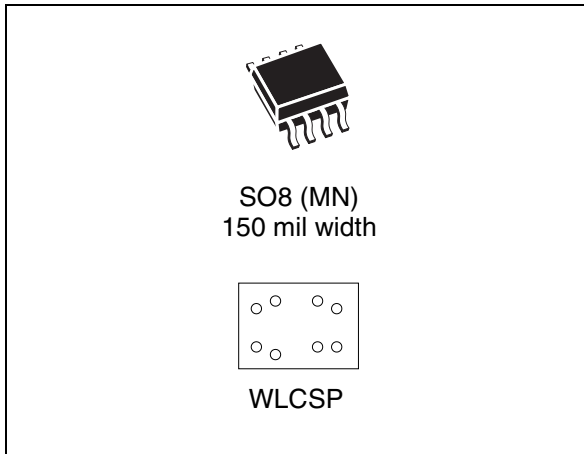


2-Mbit serial I²C bus EEPROM

Datasheet - production data

**Features**

- Compatible with all I²C bus modes:
 - 1 MHz
 - 400 kHz
 - 100 kHz
- Memory array:
 - 2 Mbit (256 Kbytes) of EEPROM
 - Page size: 256 bytes
 - Additional Write lockable page
- Single supply voltage:
 - 1.8 V to 5.5 V over –40 °C / +85 °C
- Write:
 - Byte Write within 10 ms
 - Page Write within 10 ms
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-year data retention

Packages

- SO8 ECOPACK2[®]
- WLCSP ECOPACK2[®]

Contents

1	Description	6
2	Signal description	8
2.1	Serial Clock (SCL)	8
2.2	Serial Data (SDA)	8
2.3	Chip Enable (E2)	8
2.4	Write Control (\overline{WC})	8
2.5	V _{SS} (ground)	9
2.6	Supply voltage (V _{CC})	9
2.6.1	Operating supply voltage (V _{CC})	9
2.6.2	Power-up conditions	9
2.6.3	Device reset	9
2.6.4	Power-down conditions	9
3	Memory organization	10
4	Device operation	11
4.1	Start condition	12
4.2	Stop condition	12
4.3	Data input	12
4.4	Acknowledge bit (ACK)	12
4.5	Device addressing	13
5	Instructions	14
5.1	Write operations	14
5.1.1	Byte Write	15
5.1.2	Page Write	16
5.1.3	Write Identification Page	17
5.1.4	Lock Identification Page	17
5.1.5	ECC (Error Correction Code) and Write cycling	17
5.1.6	Minimizing Write delays by polling on ACK	18
5.2	Read operations	19
5.2.1	Random Address Read	20

5.2.2	Current Address Read	20
5.2.3	Sequential Read	20
5.2.4	Read Identification Page	20
5.2.5	Read the lock status	21
6	Initial delivery state	21
7	Maximum rating	22
8	DC and AC parameters	23
9	Package mechanical data	30
10	Part numbering	34
11	Revision history	35

List of tables

Table 1.	Signal names	6
Table 2.	Device select code	13
Table 3.	Most significant address byte	14
Table 4.	Least significant address byte	14
Table 5.	Absolute maximum ratings	22
Table 6.	Operating conditions	23
Table 7.	AC measurement conditions	23
Table 8.	Input parameters	23
Table 9.	Cycling performance	24
Table 10.	Memory cell data retention	24
Table 11.	DC characteristics	25
Table 12.	400 kHz AC characteristics	26
Table 13.	1 MHz AC characteristics	27
Table 14.	SO8N – 8-lead plastic small outline, 150 mils body width, package data	31
Table 15.	M24M02-DR WLCSP package mechanical data	32
Table 16.	Ordering information scheme	34
Table 17.	Document revision history	35

List of figures

Figure 1.	Logic diagram	6
Figure 2.	SO8 connections, top view	6
Figure 3.	WLCSP connections	7
Figure 4.	Chip enable inputs connection	8
Figure 5.	Block diagram	10
Figure 6.	I ² C bus protocol	11
Figure 7.	Write mode sequences with $\overline{WC} = 0$ (data write enabled)	15
Figure 8.	Write mode sequences with $\overline{WC} = 1$ (data write inhibited)	16
Figure 9.	Write cycle polling flowchart using ACK	18
Figure 10.	Read mode sequences	19
Figure 11.	AC measurement I/O waveform	23
Figure 12.	Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I ² C bus at maximum frequency $f_C = 400$ kHz	28
Figure 13.	Maximum R_{bus} value versus bus parasitic capacitance C_{bus} for an I ² C bus at maximum frequency $f_C = 1$ MHz	28
Figure 14.	AC waveforms	29
Figure 15.	SO8N – 8-lead plastic small outline, 150 mils body width, package outline	31
Figure 16.	M24M02-DR WLCSP package outline, bump side view	32
Figure 17.	M24M02-DR WLCSP recommended footprint	33

1 Description

The M24M02-DR is a 2 Mb I²C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 256 K × 8 bits.

The M24M02-DR can operate with a supply voltage from 1.8 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

The M24M02-DR offers an additional page, named the Identification Page (256 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

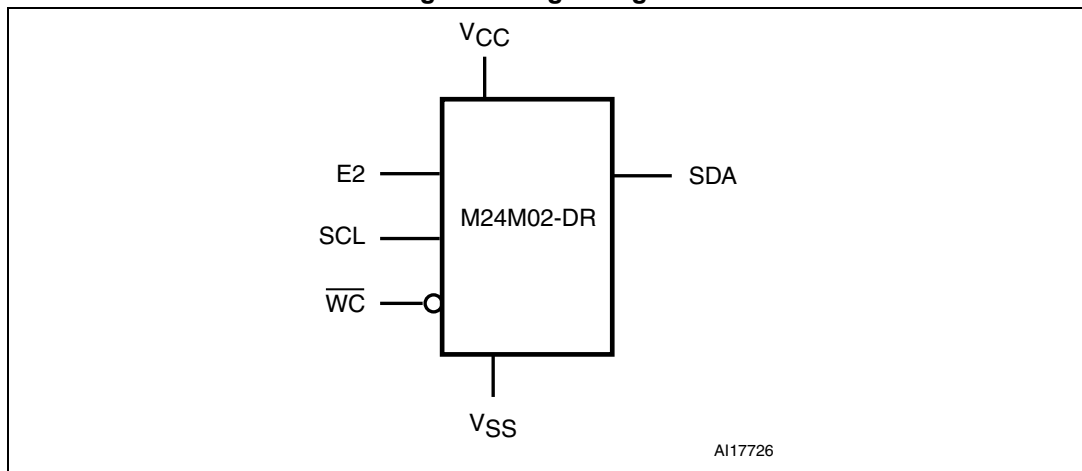
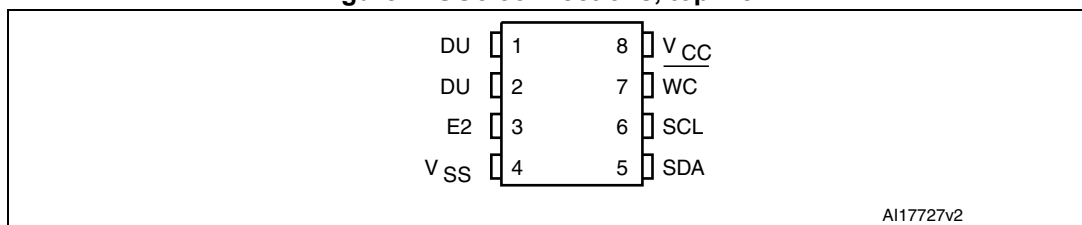


Table 1. Signal names

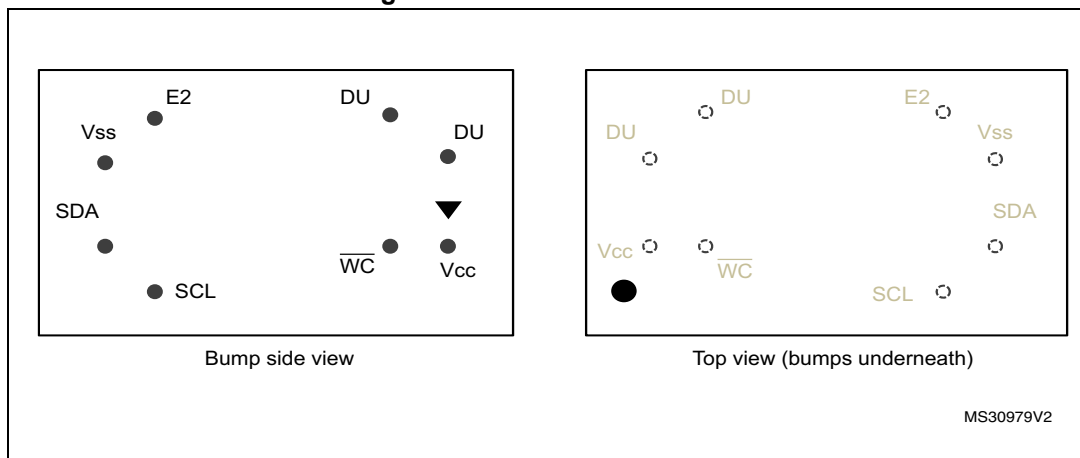
Signal name	Function	Direction
E2	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
\overline{WC}	Write Control	Input
V _{CC}	Supply voltage	-
V _{SS}	Ground	-

Figure 2. SO8 connections, top view



1. DU: Don't Use (if connected, must be connected to V_{SS})
2. See [Section 9: Package mechanical data](#) for package dimensions, and how to identify pin 1

Figure 3. WLCSP connections



1. DU: Don't Use (must be left floating)
2. See [Section 9: Package mechanical data](#) for package dimensions, and how to identify pin 1.

2 Signal description

2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

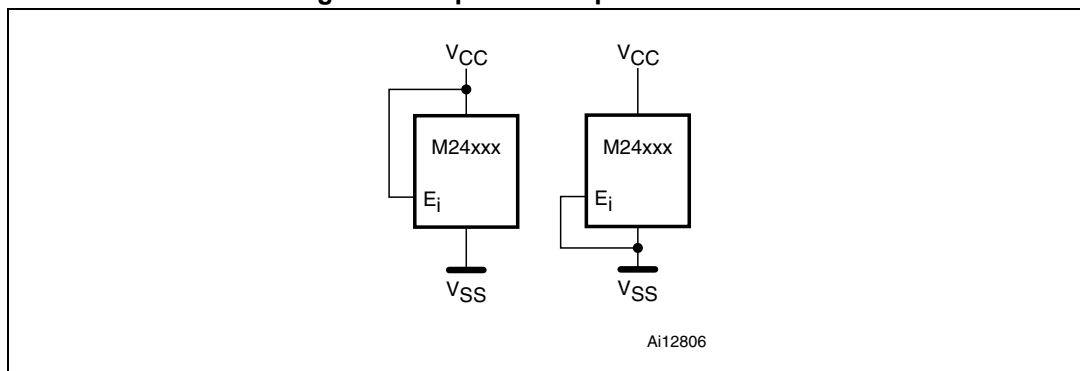
2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected ([Figure 12](#) indicates how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2)

This input signal is used to set the value that is to be looked for on the bit b3 of the 7-bit device select code. This input must be tied to V_{CC} or V_{SS} , to establish the device select code as shown in [Figure 4](#). When not connected (left floating), this input is read as low (0).

Figure 4. Chip enable inputs connection



2.4 Write Control (\overline{WC})

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control (\overline{WC}) is driven high. Write operations are enabled when Write Control (\overline{WC}) is either driven low or left floating.

When Write Control (\overline{WC}) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range must be applied (see Operating conditions in [Section 8: DC and AC parameters](#)). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in [Section 8: DC and AC parameters](#)) and the rise time must not vary faster than 1 V/ μ s.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in [Section 8: DC and AC parameters](#)). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range (see Operating conditions in [Section 8: DC and AC parameters](#)).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below $V_{CC}(\min)$. When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

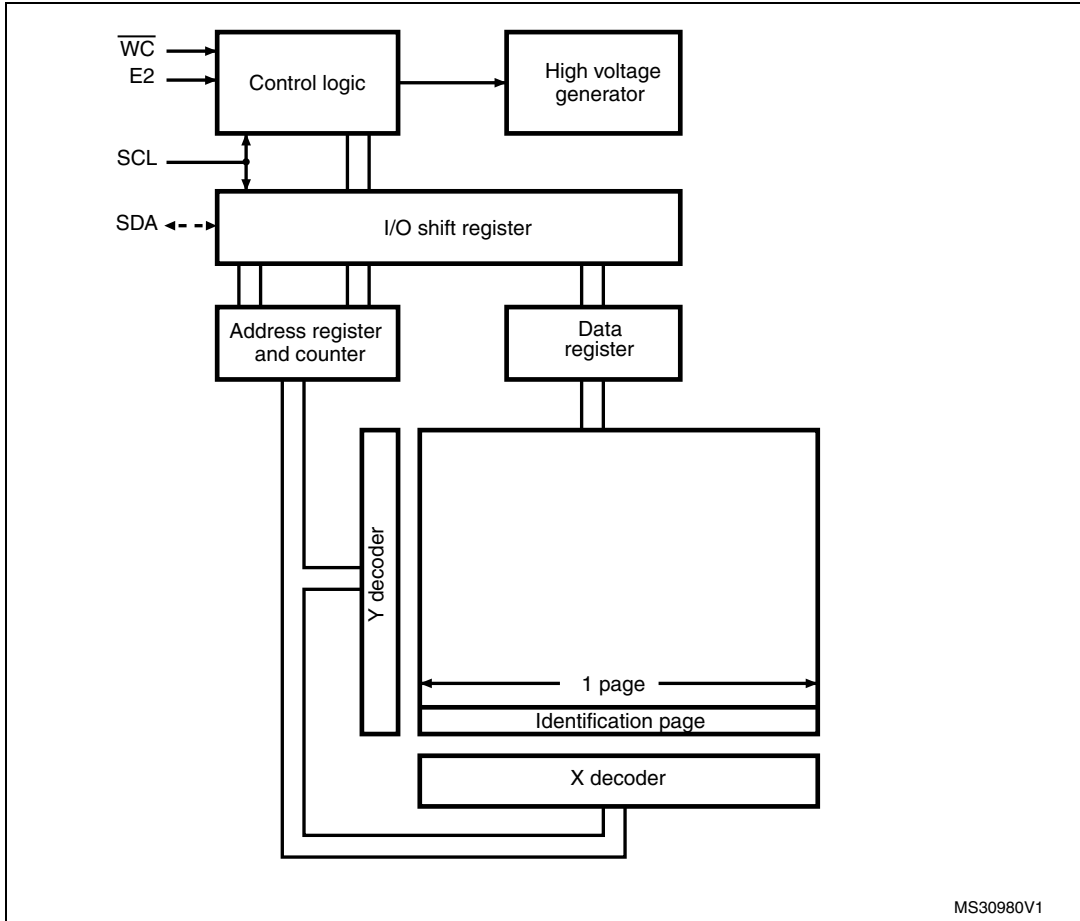
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

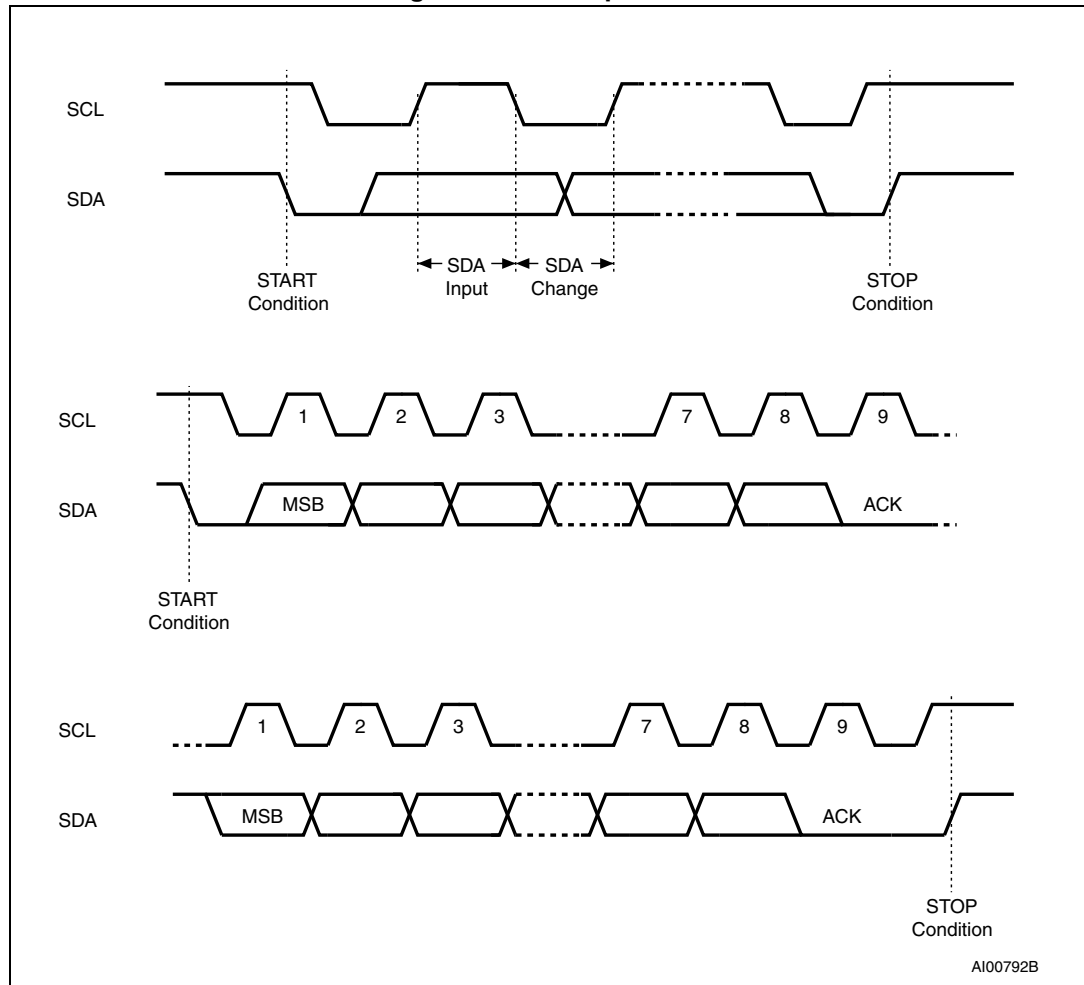
Figure 5. Block diagram



4 Device operation

The device supports the I²C protocol. This is summarized in [Figure 6](#). Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 6. I²C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in [Table 2](#) (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

	Device type identifier ⁽¹⁾				Chip Enable	MSB address bits		\overline{RW}
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2 ⁽²⁾	A17	A16	\overline{RW}
Device select code when addressing the Identification page	1	0	1	1	E2 ⁽²⁾	X	X	\overline{RW}

1. The most significant bit, b7, is sent first.

2. E2 bit value is compared to the logic level applied on the input pin E2.

When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E2) input.

The 8th bit is the Read/Write bit (\overline{RW}). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the $\overline{R/\overline{W}}$ bit (\overline{RW}) reset to 0. The device acknowledges this, as shown in [Figure 7](#), and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8
-----	-----	-----	-----	-----	-----	----	----

Table 4. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0
----	----	----	----	----	----	----	----

The 256 Kbytes (2 Mb) are addressed with 18 address bits, the 16 lower address bits being defined by the two address bytes and the most significant address bits (A17, A16) being included in the Device Select code (see [Table 4](#)).

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

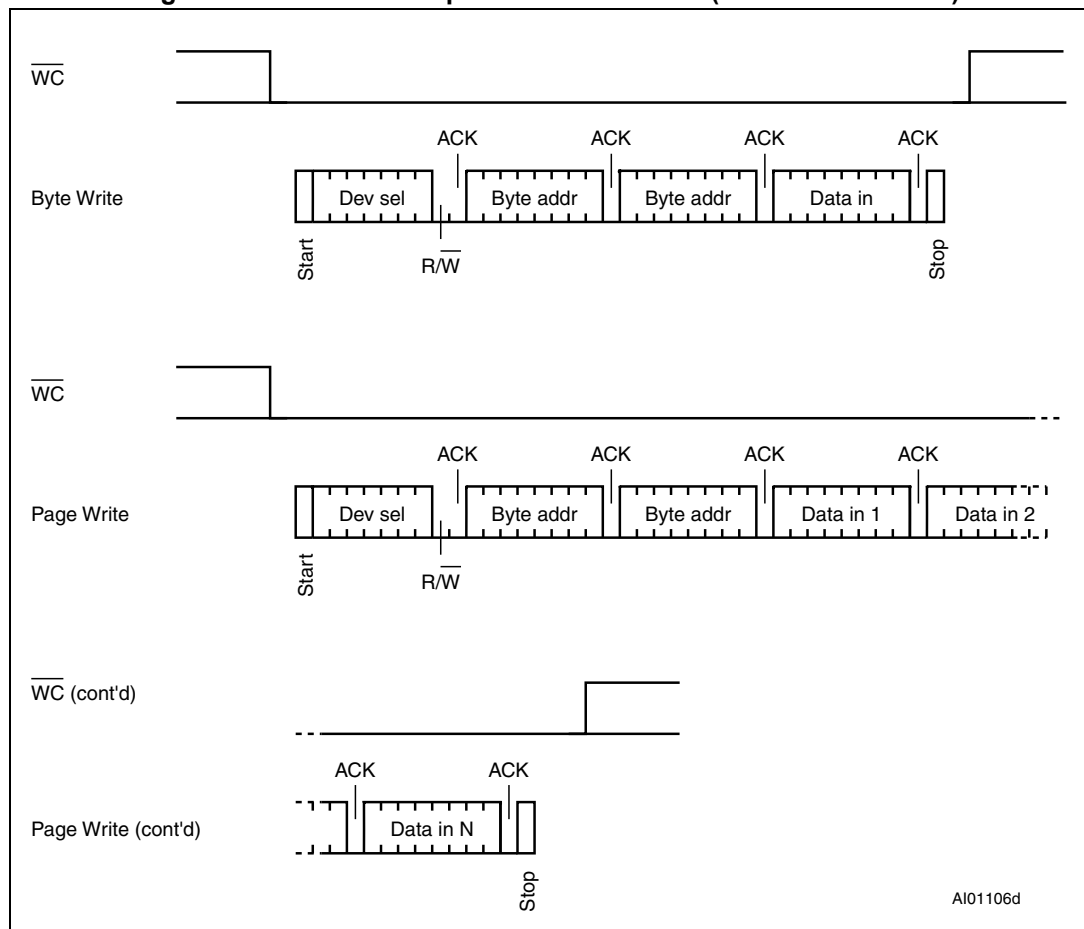
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in [Figure 8](#).

5.1.1 Byte Write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control (\overline{WC}) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 7*.

Figure 7. Write mode sequences with $\overline{WC} = 0$ (data write enabled)



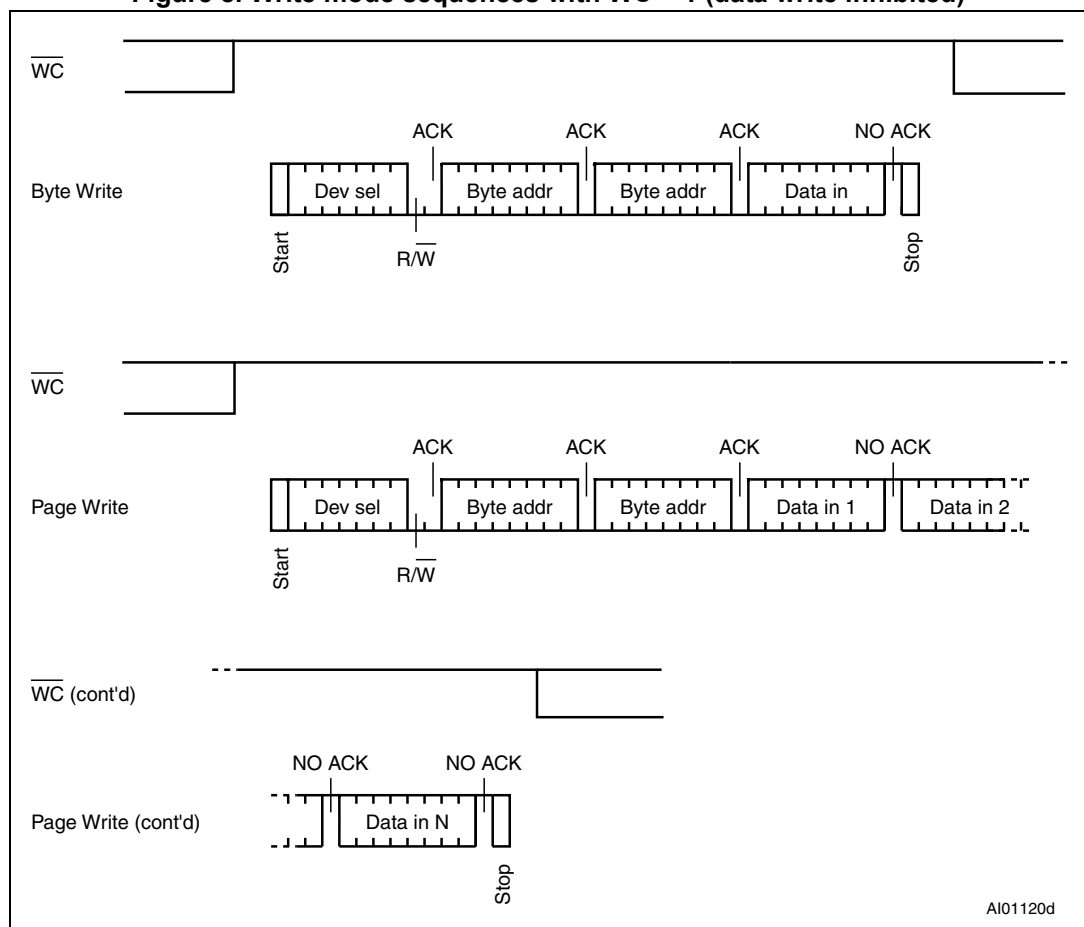
5.1.2 Page Write

The Page Write mode allows up to 256 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A17/A8, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 256 bytes of data, each of which is acknowledged by the device if Write Control (\overline{WC}) is low. If Write Control (\overline{WC}) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in [Figure 8](#). After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 8. Write mode sequences with $\overline{WC} = 1$ (data write inhibited)



AI01120d

5.1.3 Write Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A17/A8 are don't care except for address bit A10 which must be '0'. LSB address bits A7/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

5.1.4 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

5.1.5 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I²C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes⁽¹⁾. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group⁽¹⁾. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined [Table 9: Cycling performance](#).

1. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

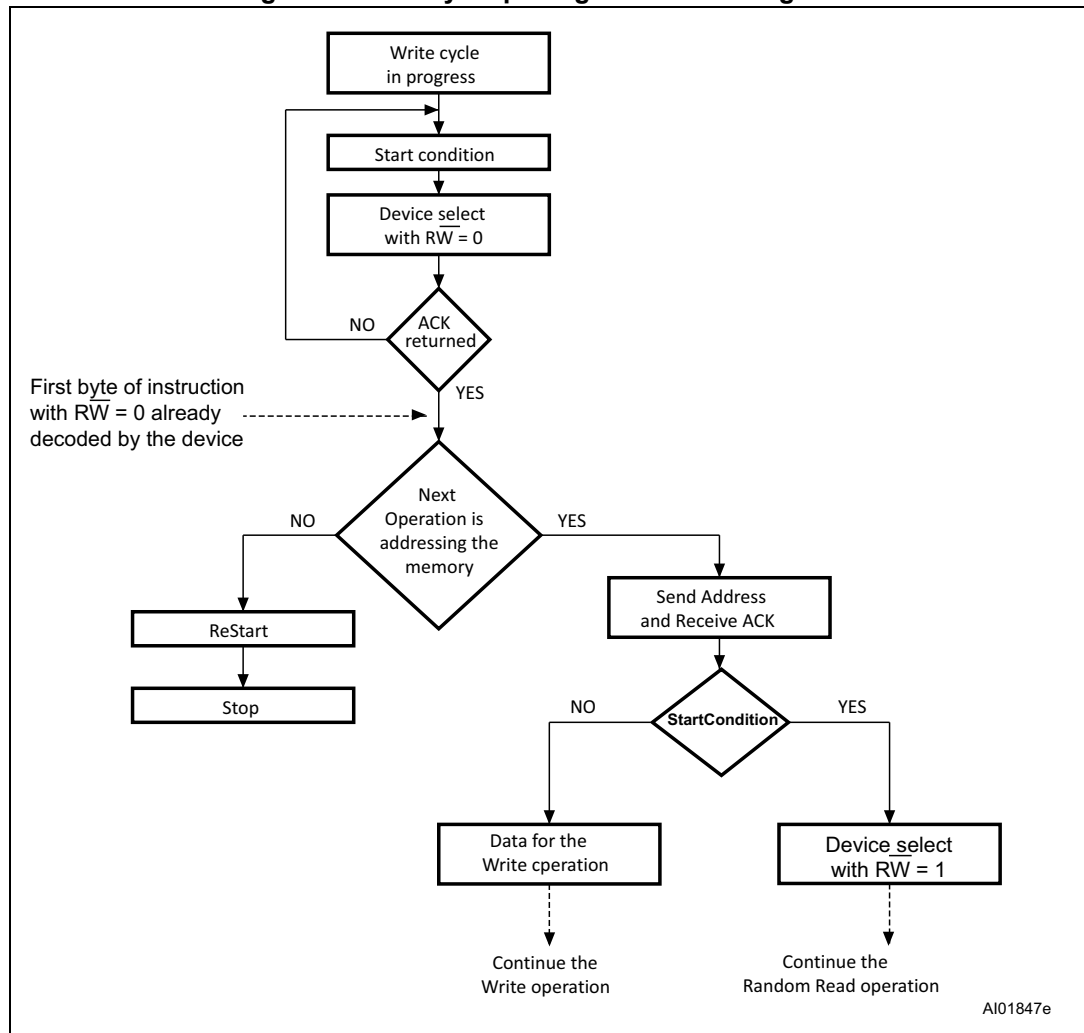
5.1.6 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in [Section 8: DC and AC parameters](#), but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in [Figure 9](#), is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Write cycle polling flowchart using ACK



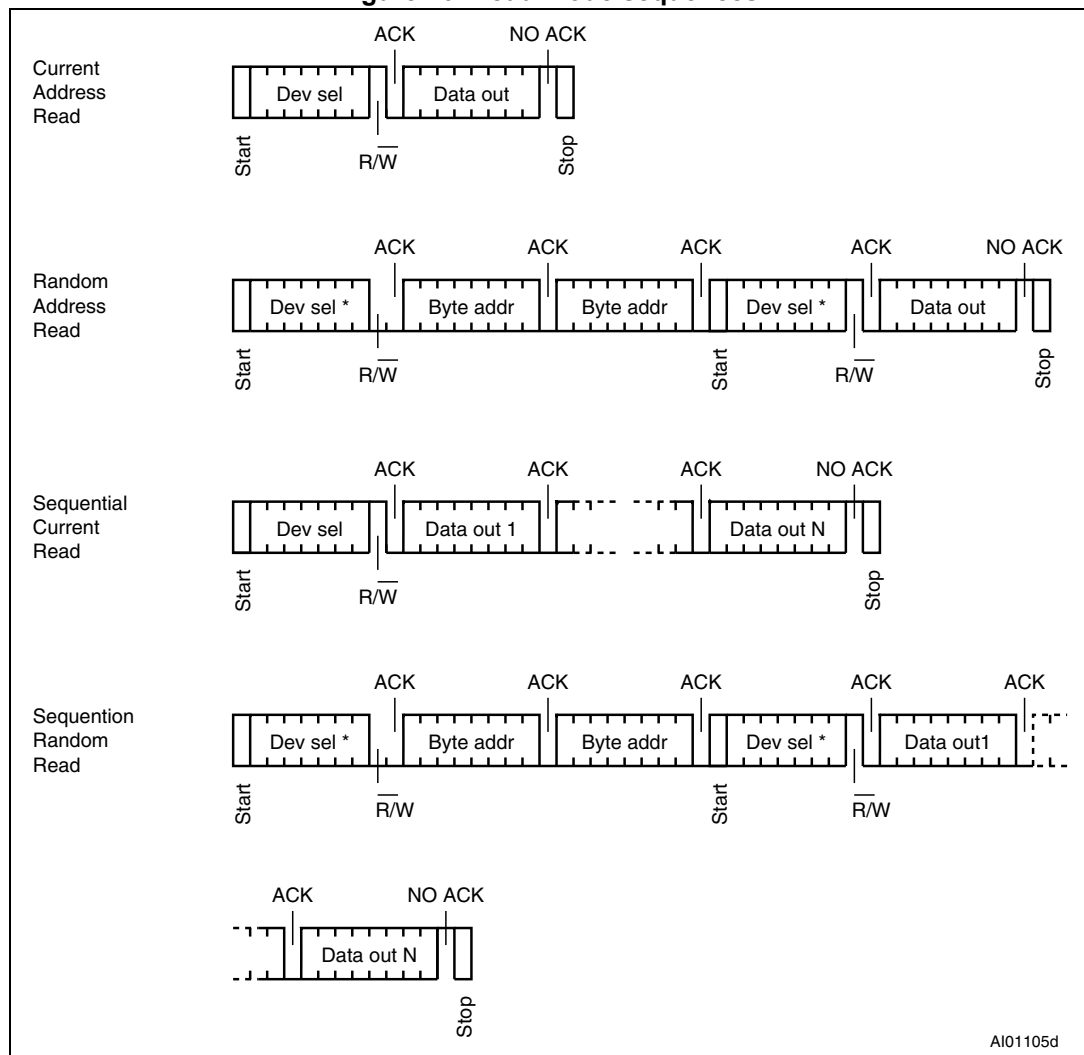
1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

5.2 Read operations

Read operations are performed independently of the state of the Write Control (\overline{WC}) signal. After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 10. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in [Figure 10](#)) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the \overline{RW} bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the \overline{RW} bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in [Figure 10](#), *without* acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the Identification page. When accessing the Identification page, the address counter value is loaded with the byte location in the Identification page, therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory, see [Section 5.2.1](#)) instead of the Current Address Read instruction.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in [Figure 10](#).

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.2.4 Read Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A17/A8 are don't care, the LSB address bits A7/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 100d, the number of bytes should be less than or equal to 156, as the ID page boundary is 256 bytes).

5.2.5 Read the lock status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

6 Initial delivery state

The device is delivered with all the memory array bits and Identification page bits set to 1 (each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in [Table 5](#) may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	-40	130	°C
T _{STG}	Storage temperature	-65	150	°C
T _{LEAD}	Lead temperature during soldering	see note ⁽¹⁾		°C
I _{OL}	DC output current (SDA = 0)	-	5	mA
V _{IO}	Input or output range	-0.50	6.5	V
V _{CC}	Supply voltage	-0.50	6.5	V
V _{ESD}	Electrostatic pulse (Human Body model) ⁽²⁾	-	3000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω).

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 6. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	-40	85	°C

Table 7. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time	-	50	ns
	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 11. AC measurement I/O waveform

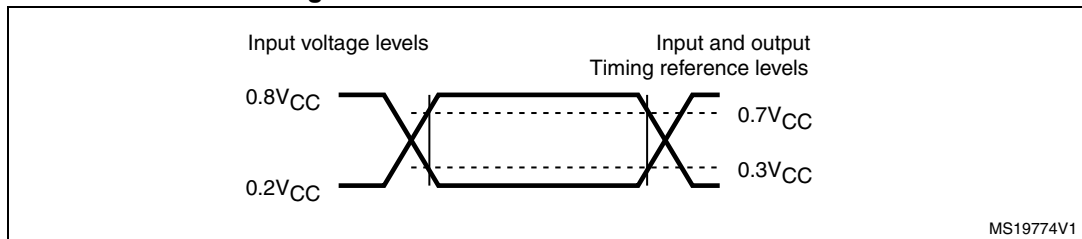


Table 8. Input parameters

Symbol	Parameter ⁽¹⁾	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_L	Input impedance ($E2\overline{WC}$) ⁽²⁾	$V_{IN} < 0.3 V_{CC}$	30	-	k Ω
Z_H		$V_{IN} > 0.7 V_{CC}$	500	-	k Ω

1. Characterized only, not tested in production.
2. E2 input impedance when the memory is selected (after a Start condition).

Table 9. Cycling performance

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance ⁽¹⁾	$T_A \leq 25\text{ °C}, V_{CC}(\text{min}) < V_{CC} < V_{CC}(\text{max})$	4,000,000	Write cycle ⁽²⁾
		$T_A = 85\text{ °C}, V_{CC}(\text{min}) < V_{CC} < V_{CC}(\text{max})$	1,200,000	

1. The write cycle endurance is defined for group of four bytes located at addresses $[4*N, 4*N+1, 4*N+2, 4*N+3]$ where N is an integer. The Write cycle endurance is defined by characterization and qualification.
2. A Write cycle is executed when either a Page Write, a Byte write, a Write Identification Page or a Lock Identification Page instruction is decoded. When using the Byte Write, the Page Write or the Write Identification Page, refer also to [Section 5.1.5: ECC \(Error Correction Code\) and Write cycling](#)

Table 10. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention ⁽¹⁾	$T_A = 55\text{ °C}$	200	Year

1. For products identified by process letter K. The data retention behavior is checked in production, while the 200-year limit is defined from characterization and qualification results.

Table 11. DC characteristics

Symbol	Parameter	Test conditions (in addition to those in Table 6 and Table 7)	Min.	Max.	Unit
I_{LI}	Input leakage current (E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode	-	± 2	μA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	μA
I_{CC}	Supply current (Read)	$V_{CC} = 1.8 V, f_c = 400 kHz$	-	1	mA
		$V_{CC} = 2.5 V, f_c = 400 kHz$	-	1	mA
		$V_{CC} = 5.5 V, f_c = 400 kHz$	-	2	mA
		$1.8 V < V_{CC} < 5.5 V, f_c = 1 MHz$	-	2.5	mA
I_{CC0}	Supply current (Write)	Average value during t_w , $1.8 V \leq V_{CC} \leq 5.5 V$	-	2 ⁽¹⁾	mA
I_{CC1}	Standby supply current	Device not selected ⁽²⁾ , $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 1.8 V$	-	3	μA
		Device not selected ⁽²⁾ , $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5 V$	-	5	μA
		Device not selected ⁽²⁾ , $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5.5 V$	-	5	μA
V_{IL}	Input low voltage (SCL, SDA, WC)	$1.8 V \leq V_{CC} < 2.5 V$	-0.45	$0.25 V_{CC}$	V
		$2.5 V \leq V_{CC} < 5.5 V$	-0.45	$0.30 V_{CC}$	V
V_{IH}	Input high voltage (SCL, SDA, WC)	$1.8 V \leq V_{CC} < 2.5 V$	$0.75 V_{CC}$	$V_{CC}+1$	V
		$2.5 V \leq V_{CC} < 5.5 V$	$0.70 V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 1.0 mA, V_{CC} = 1.8 V$	-	0.2	V
		$I_{OL} = 2.1 mA, V_{CC} = 2.5 V$	-	0.4	V
		$I_{OL} = 3.0 mA, V_{CC} = 5.5 V$	-	0.4	V

1. Characterized only, not tested in production.

2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_w (t_w is triggered by the correct decoding of a Write instruction).

Table 12. 400 kHz AC characteristics

Symbol	Alt.	Parameter ⁽¹⁾	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
$t_{QL1QL2}^{(2)}$	t_F	SDA (out) fall time	20 ⁽³⁾	120	ns
t_{XH1XH2}	t_R	Input signal rise time	(4)	(4)	ns
t_{XL1XL2}	t_F	Input signal fall time	(4)	(4)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
$t_{CLQX}^{(5)}$	t_{DH}	Data out hold time	100	-	ns
$t_{CLQV}^{(6)}$	t_{AA}	Clock low to next data valid (access time)	100-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
$t_{WLDL}^{(7)}$	$t_{SU:WC}$	\overline{WC} set up time (before the Start condition)	0	-	μ s
$t_{DHWL}^{(8)}$	$t_{HD:WC}$	\overline{WC} hold time (after the Stop condition)	1	-	μ s
t_W	t_{WR}	Write time	-	10	ms
$t_{NS}^{(2)}$		Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

1. Test conditions (in addition to those specified under Operating conditions and AC test measurement conditions in [Section 8: DC and AC parameters](#)).
2. Characterized only, not tested in production.
3. With $C_L = 10$ pF.
4. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when $f_C < 400$ kHz.
5. The min value for t_{CLQX} (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3 V_{CC}$ or $0.7 V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in [Figure 12](#).
7. $\overline{WC}=0$ set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}=0$ hold time condition to enable the execution of a WRITE command.

Table 13. 1 MHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	400	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(1)	(1)	ns
t_{XL1XL2}	t_F	Input signal fall time	(1)	(1)	ns
$t_{QL1QL2}^{(2)}$	t_F	SDA (out) fall time	20 ⁽³⁾	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
$t_{CLQX}^{(4)}$	t_{DH}	Data out hold time	100	-	ns
$t_{CLQV}^{(5)}$	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
$t_{WLDL}^{(6)}$	$t_{SU:WC}$	\overline{WC} set up time (before the Start condition)	0	-	μ s
$t_{DHWL}^{(7)(2)}$	$t_{HD:WC}$	\overline{WC} hold time (after the Stop condition)	1	-	μ s
t_W	t_{WR}	Write time	-	10	ms
$t_{NS}^{(2)}$		Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when $f_C < 1$ MHz.
2. Characterized only, not tested in production.
3. With $C_L = 10$ pF.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3 V_{CC}$ or $0.7 V_{CC}$, assuming that the $R_{bus} \times C_{bus}$ time constant is within the values specified in [Figure 13](#).
6. $\overline{WC}=0$ set up time condition to enable the execution of a WRITE command.
7. $\overline{WC}=0$ hold time condition to enable the execution of a WRITE command.

Figure 12. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I²C bus at maximum frequency $f_C = 400$ kHz

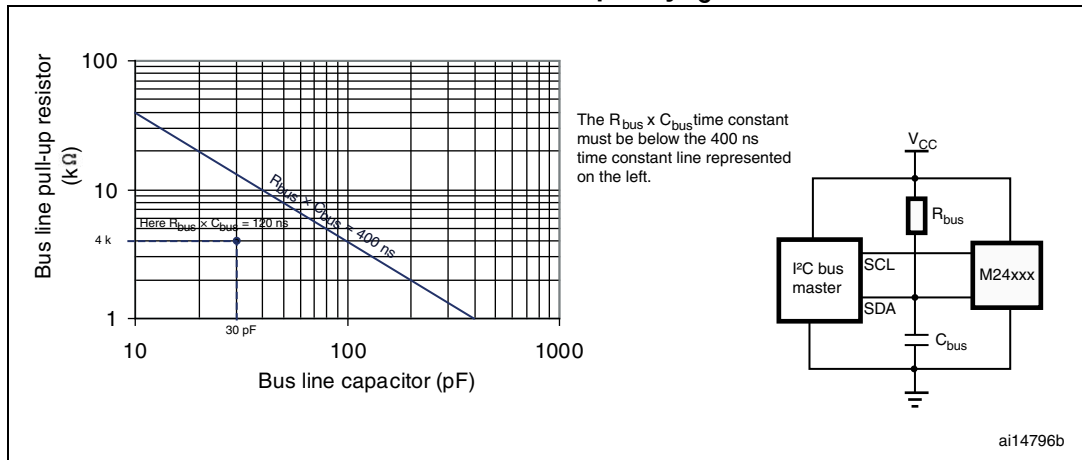


Figure 13. Maximum R_{bus} value versus bus parasitic capacitance C_{bus}) for an I²C bus at maximum frequency $f_C = 1$ MHz

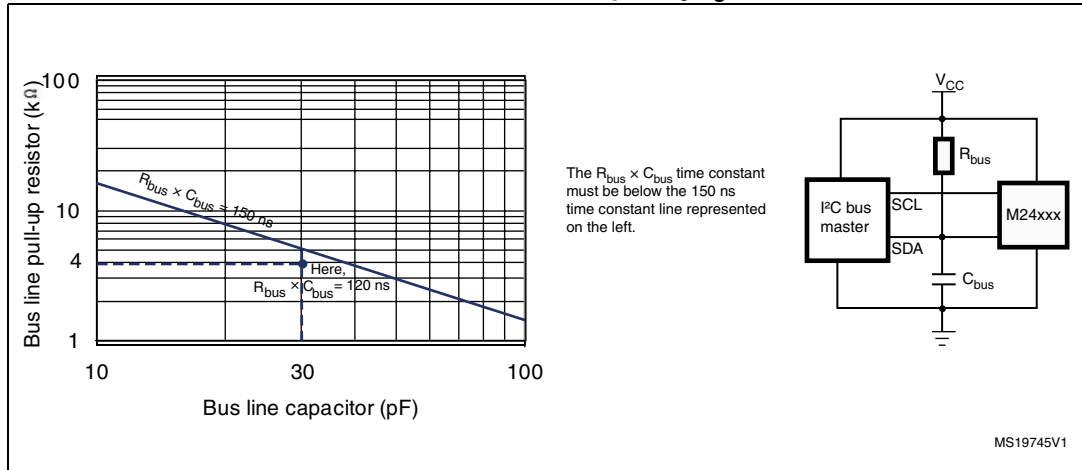
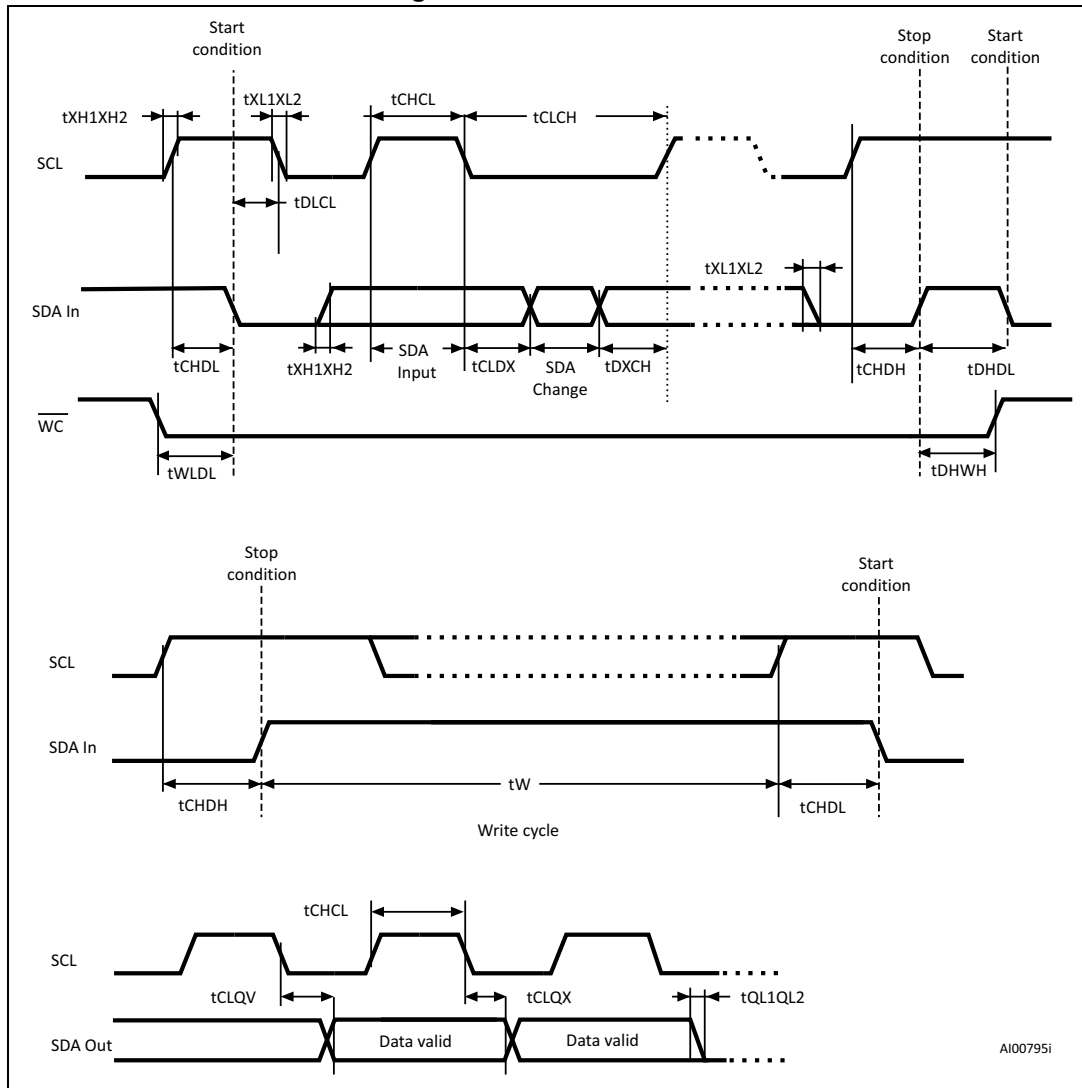


Figure 14. AC waveforms

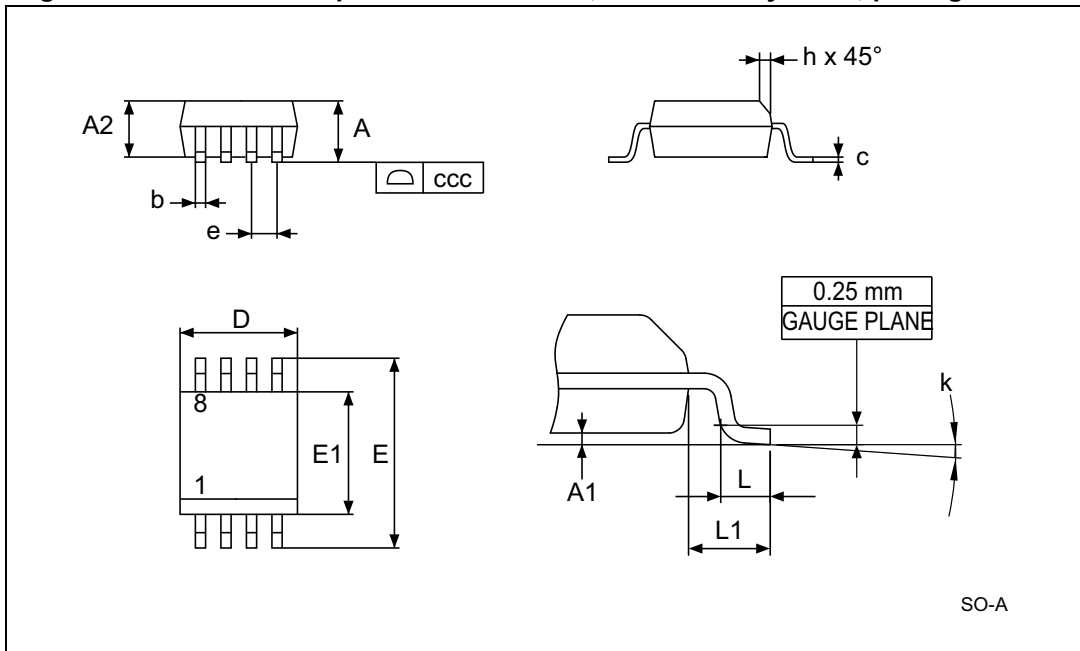


A100795i

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 15. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



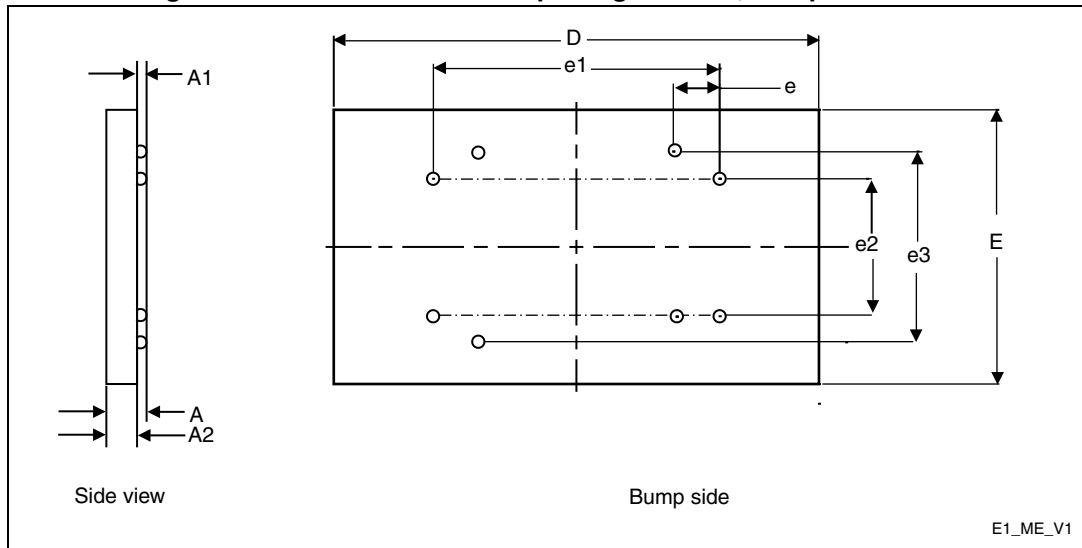
1. Drawing is not to scale.

Table 14. SO8N – 8-lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.750	–	–	0.0689
A1	–	0.100	0.250	–	0.0039	0.0098
A2	–	1.250	–	–	0.0492	–
b	–	0.280	0.480	–	0.0110	0.0189
c	–	0.170	0.230	–	0.0067	0.0091
ccc	–	–	0.100	–	–	0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	–	–	0.0500	–	–
h	–	0.250	0.500	–	0.0098	0.0197
k	–	0°	8°	–	0°	8°
L	–	0.400	1.270	–	0.0157	0.0500
L1	1.040	–	–	0.0409	–	–

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 16. M24M02-DR WLCSP package outline, bump side view



1. Drawing is not to scale.

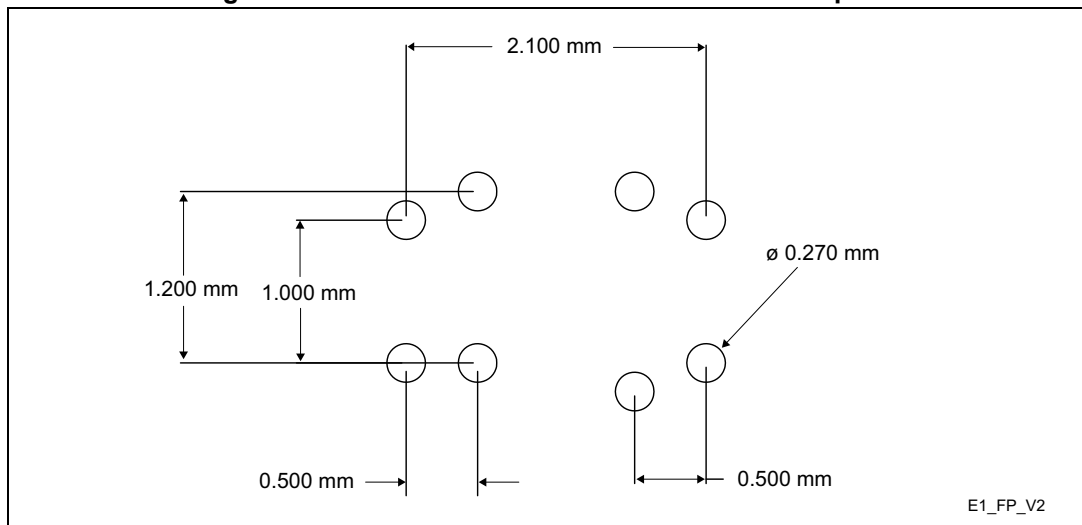
Table 15. M24M02-DR WLCSP package mechanical data⁽¹⁾

Symbol	millimeters			inches ⁽²⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.500	0.580	0.0213	0.0197	0.0228
A1	0.190	-	-	0.0075	-	-
A2	0.350	-	-	0.0138	-	-
B (ball diameter)	0.270	-	-	0.0106	-	-
D	3.536	3.556	3.576	0.1392	0.1400	0.1408
E	1.991	2.011	2.031	0.0784	0.0792	0.0800
e	-	0.500	-	-	0.0197	-
e1	-	2.100	-	-	0.0827	-
e2	-	1.000	-	-	0.0394	-
e3	-	1.400	-	-	0.0551	-

1. Preliminary data.

2. Values in inches are converted from mm and rounded to four decimal digits.

Figure 17. M24M02-DR WLCSP recommended footprint



10 Part numbering

Table 16. Ordering information scheme

Example:	M24M02-D	R	MN	6	T	P	/K
Device type M24 = I ² C serial access EEPROM							
Device function M02-D = 2 Mbit (256 Kb × 8 bits) EEPROM with additional identification page							
Operating voltage R = V _{CC} = 1.8 V to 5.5 V							
Package MN = SO8 (150 mil width) ⁽¹⁾ CS = Standard WLCSP ⁽¹⁾							
Device grade 6 = Industrial: device tested with standard test flow over -40 to 85 °C							
Option T = Tape and reel packing blank = tube packing							
Plating technology P = ECOPACK [®] (RoHS compliant)							
Process⁽²⁾ /K = Manufacturing technology code							

1. RoHS-compliant and halogen-free (ECOPACK2[®])
2. The process letters apply to WLCSP devices only. The process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

11 Revision history

Table 17. Document revision history

Date	Revision	Changes
22-Dec-2010	1	Initial release.
09-Feb-2011	2	Updated: <ul style="list-style-type: none"> – Section 3.18: Read Identification Page – Section 3.19: Read the lock status – Figure 2: SO8 connections – Table 6: Absolute maximum ratings – Table 10: Input parameters – Table 11: DC characteristics – Table 12: AC characteristics at 400 kHz – Table 13: 1 MHz AC characteristics Deleted: <ul style="list-style-type: none"> – Table 15 “Available M24M02-x products (package, voltage range, frequency, temperature grade)”.
09-Aug-2011	3	Updated Figure 5: Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I2C bus at maximum frequency $f_C = 1$ MHz and Table 11: DC characteristics .
07-Feb-2012	4	Updated: <ul style="list-style-type: none"> – Table 2: Device select code – Table 3: Most significant address byte – Table 4: Least significant address byte. – Section 3.6: Write operations – Section 3.8: Page Write
25-Oct-2012	5	Updated document template and text (minor changes). Cycling updated to 4 million cycles and data retention updated to 200 years. Added WLCSP packages.
04-Jun-2013	6	Document reformatted. Removed information related to thin WLCSP package. Updated: <ul style="list-style-type: none"> – WLCSP package silhouette on cover page – Section 1: Description – Figure 3: WLCSP connections – Note ⁽¹⁾ under Table 5: Absolute maximum ratings. Added Figure 17: M24M02-DR WLCSP recommended footprint
23-May-2014	7	removed note on page 7, Updated Table 2: Device select code , updated section numbering for Section 5.2.4 and Section 5.2.5 , updated note 1 on Table 10: Memory cell data retention , updated Figure 17: M24M02-DR WLCSP recommended footprint .

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com